LISTING OF CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the Application:

Claims 1-14 (canceled)

Claim 15 (original): In a process for fabricating a semiconductor memory, a process of forming a capacitor on a semiconductor substrate, comprising the steps of:

forming a barrier layer having a lower surface connected to an upper end of a conducting member having a lower end connected to an underlying layer;

forming a lower electrode on said barrier layer;

forming a dielectric film on said lower electrode; and

forming an upper electrode on said dielectric film,

wherein said step of forming said barrier layer includes the step of forming a first metal film, a metal nitride film and a second metal film in the named order.

Claim 16 (original): A process for fabricating a semiconductor memory, claimed in Claim 15,

wherein said conducting member is formed in an interlayer insulator film formed on said semiconductor substrate, said upper end of said conducting member reaching a surface of said interlayer insulator film, and said lower end of said conducting member reaching a underlying conducting layer or a surface of said semiconductor substrate,

wherein said capacitor is formed by depositing said barrier layer, said lower electrode, said dielectric layer and said upper electrode on said surface of said interlayer insulator film in the named order to form a laminated film, and by patterning the laminated film so as to form said capacitor having said lower electrode electrically connected through said barrier layer to said conducting member, and

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wherein said step of forming said barrier layer includes the steps of:

forming said first metal film on said surface of said interlayer insulator film to form a lowermost layer of said barrier layer;

forming said metal nitride film on said first metal film; and

forming said second metal film on said metal nitride film to form an uppermost layer of said barrier layer.

Claim 17 (original): A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said metal nitride film is formed of a nitride of a metal element constituting said first metal film or said second metal film.

Claim 18 (original): A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said first metal film, said metal nitride film and said second metal film are formed by one combination selected from the group consisting of:

Ti, TiN and Ti

Ti, TaN and Ta

Ta, TaN and Ti,

Pt, TiN and Ti,

Pt, TaN and Ta, and

Pt, TaN and Ti.

Claim 19 (original); A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said lower electrode is formed of at least one selected from the group consisting of Ru, Ir, Ru oxide, Ir oxide and $SrRuO_3$.

Claim 20 (original): A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said step of forming said barrier layer includes the steps of:

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forming said first metal film on said surface of said interlayer insulator film;

forming said metal nitride film on said first metal film;

forming on said metal nitride film a predetermined number of multilayer film(s) each formed of a metal film and a metal nitride film; and

forming said second metal film on said predetermined number of multilayer film(s) to form said uppermost layer of said barrier layer.

Claim 21 (original): A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said conductive member is formed of mainly W.

Claim 22 (original): A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said capacitor dielectric film is deposited at a film deposition temperature of not greater than 500 degrees Celsius.

Claim 23 (original): A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said capacitor dielectric film is deposited at a film deposition temperature of not greater than 475 degrees Celsius.

Claim 24 (original): A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said capacitor dielectric film is formed by depositing a PZT film by a chemical vapor deposition process at a substrate temperature of not greater than 430 degrees Celsius.

Claim 25 (original): A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said capacitor dielectric film is formed by a sputtering or a solgel method.

Claim 26 (canceled)

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